WBS 6.5
System

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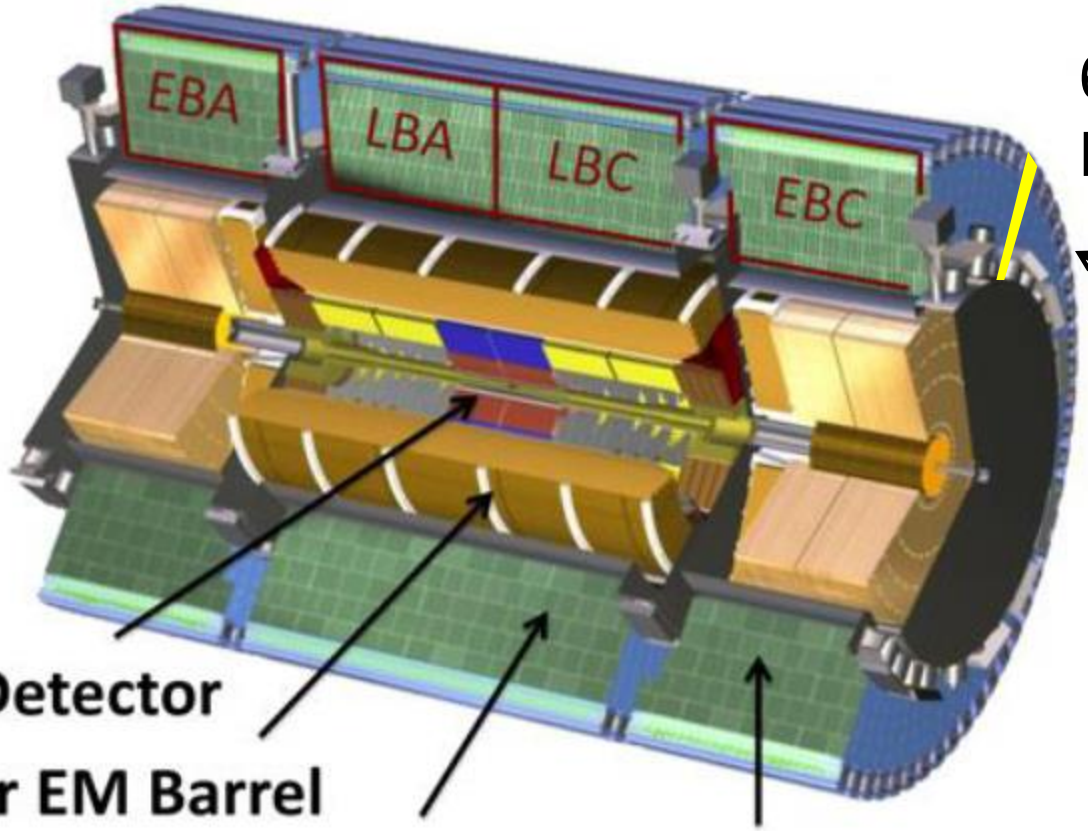
U.S. ATLAS HL-LHC Upgrade Director's Review
Brookhaven National Laboratory
Upton, New York
January 20-22, 2016

Outline

- System Overview
  - Current (Run-2) System and Motivation for Upgrade
  - ATLAS Upgrade Plans
- Proposed U.S. HL-LHC Upgrade Scope
  - Work Breakdown Structure and Contributing Institutes
  - U.S. Deliverables
- Ongoing R&D
  - Plans to Construction Project
  - Funding Needed
- Construction Project Management
  - Construction Project Budget and Schedule
  - Risk
- Closing Remarks

The Current Tile Calorimeter

4 “barrels”, 256 modules



64 ϕ Wedges
R: 2.28-3.87m

LV “finger” boxes

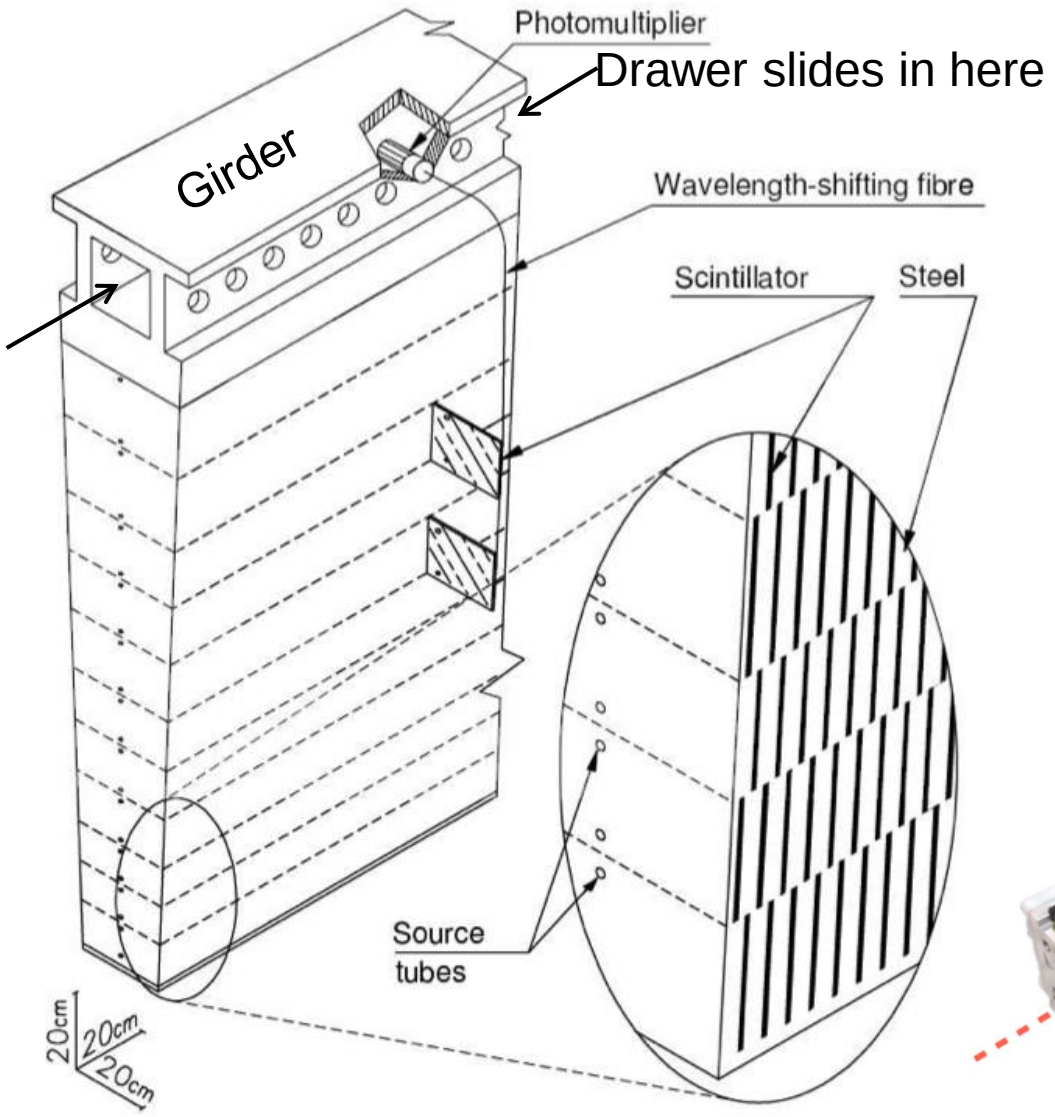
Inner Detector

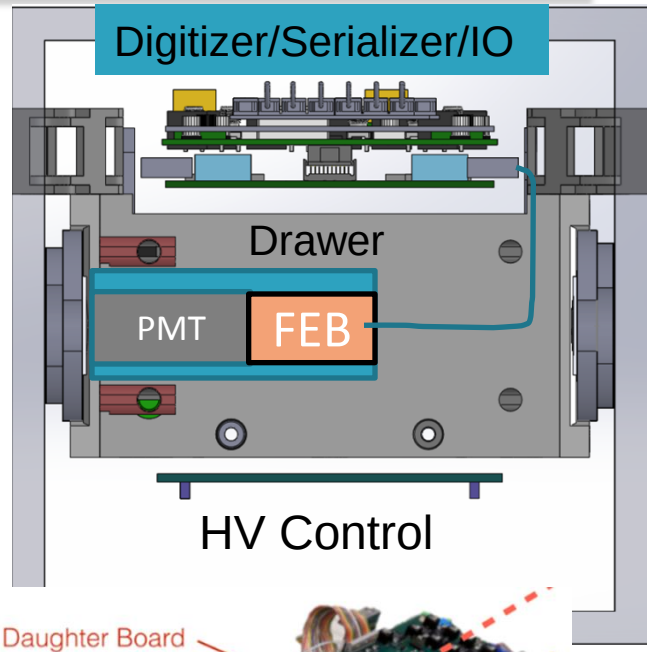
LAr EM Barrel

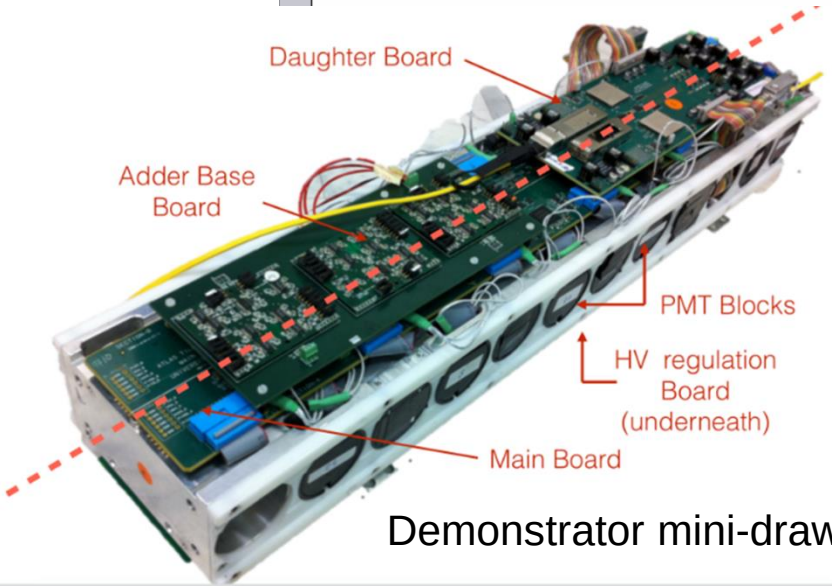
Tile Barrel

Tile Extended Barrel

Tile Wedge Structure





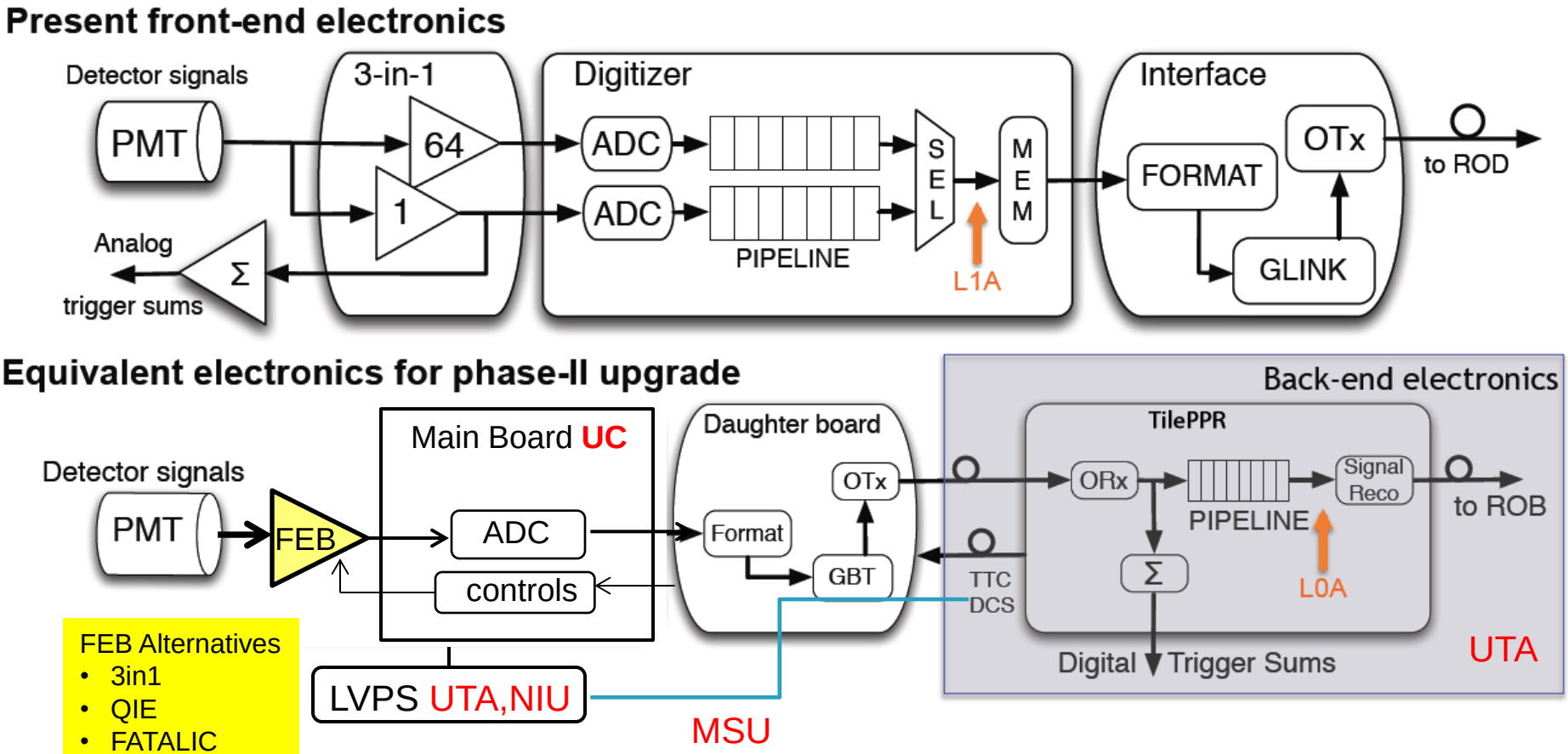


Demonstrator mini-drawer

Motivation for Upgrade

- Physics Motivation:
  - Energy resolution impacts jet rates and physics analysis:
    - ~400MeV noise on current copper trigger lines $\Rightarrow$ optical Tx
    - pileup: get better resolution by storing energies from all cells
      - get longitudinal profile too
  - Missing Energy: dead cells bad for searches
    - increase redundancy and reliability
    - reduce Single Event Upsets
  - Trigger: use information from all cells and configure smart fast triggers in back-end
  - Therefore, send all cell data off-detector: requires new front- and back-end electronics
- Technical Motivation:
  - Radiation: harden electronics, increase redundancy
    - Each drawer ϕ-half completely independent, has separate:
      - 10 volt feed, FPGA and uplink; one half can take over from the other
  - Easier and safer drawer mechanics: 69cm units instead of 140cm
  - Configurable Trigger
    - Send all cell energies to pre-processor
  - NB: the scintillator tiles and PMTs do not require upgrade

New vs Old Electronics



NB: New electronics already prototyped (“Demonstrator”)

Proposed US Scope on Tile

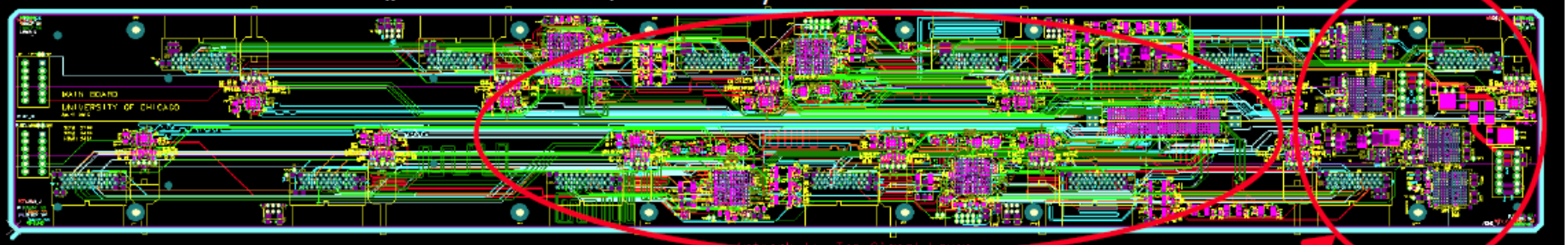
- US groups have held leadership roles in Tile since the beginning; this continues with the demonstrator R&D:
  - UChicago (UC): old and new front-end electronics
  - UTexas/Arlington (UTA): Preprocessor
  - Michigan State U (MSU): Detector Control Systems and MinBiasTrigScint
  - ANL: LVPS $\rightarrow$ shifting focus; LV taken over by UTA and Northern Illinois U
- 6.5.1.1 (UC): Main Boards of front-end system
- 6.5.2.2 (UTA-1): Pre-processor TDAQi (interface boards)
- 6.5.3.3 (MSU): motherboards for LV control
- 6.5.2.4 (UTA-2): LV Power System (50% of LV “bricks”)
- 6.5.4.4 (NIU): LV Assembly (50% of LV “boxes”)
- These US interests supported by Tile Institute Board

6.5.1.1: Main Board (UC)

- interface between FE amplifier/shaper and fast communications DaughterBoard
- 69 cm length , 16 layer board; 1024 needed
- Supplies LV levels, controls, digitization
- into 3rd prototype version for demonstrator

Complexity and Challenges:

- High speed: (640 Mbps)
- Max. trace length: (20 inches)
- All routes are same direction routes
- Crosstalk consideration: (parallel and tandem)
- Mixed signals (low noise analog and high speed digital)
- Equal timing high speed traces
- Current rate constraints
- Swish-cheesed power planes (via usage limitation)
- Many other constraints



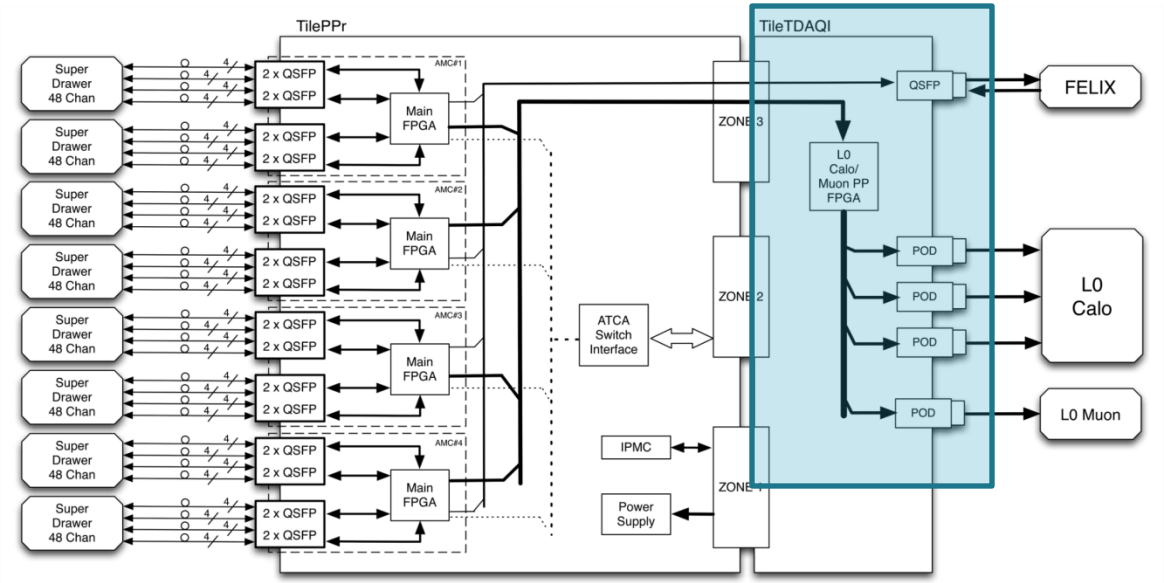
High via and trace density

High via density

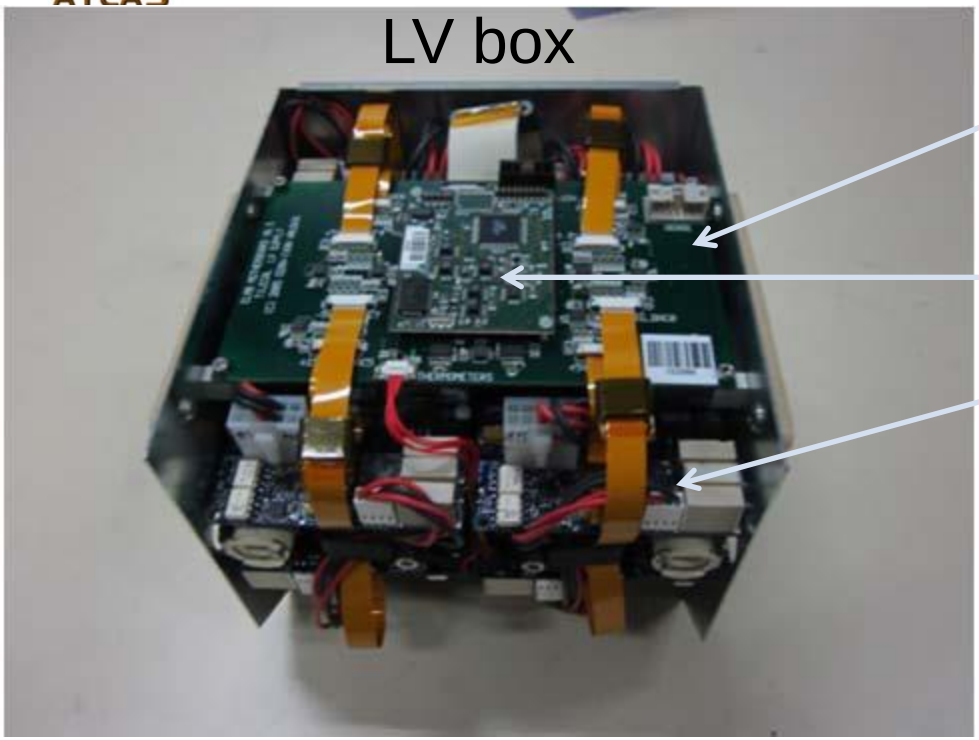
- 6 Signal layers
- 8 Power layers including 3 redundant ground layers (continuous solid plane) for signal integrity and tandem crosstalk reduction

6.5.2.2: Pre-Processor TDAQi (UTA-1)

- PPr + TDAQinterface: receive the ADC raw data, process/calibrate, route data
- TDAQi = smart rear transition module on back-end PreProcessor
  - routes processed cell data to DAQ system
  - send reduced data to trigger processors
- UTA will produce all 32 boards needed
- UTA has long involvement in sROD (PPR) maintenance, debugging
- PPR front-end prototyped for demonstrator; TDAQi designed and costed



6.5.3.3: ELMB++ Motherboard (MSU)



DCS motherboard

Embedded Local Monitor Board (ELMB):

Eight 10v “bricks”

- Motherboard with ELMB handles communication between LVbox and Detector Control System
  - set voltages
  - monitor current, temperature

- MSU proposes to design and make all 256 motherboards needed for LV system
- MSU has had longtime role in Tile control systems
- is starting work with CERN to specify ELMB++ specs

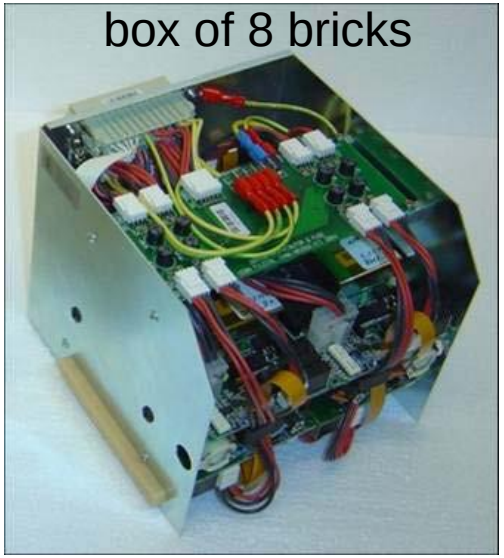
6.5.x.4: LVPS (UTA,NIU)

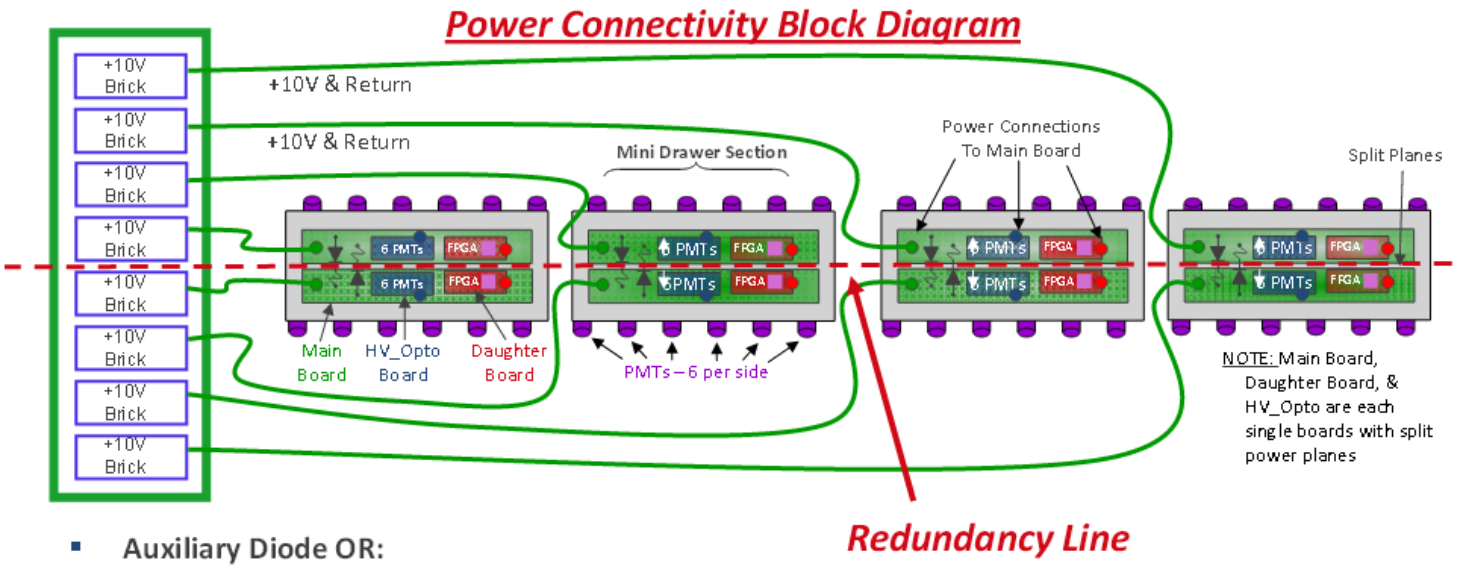
UTA makes 50% of bricks; NIU makes/assembles 50% of boxes

One 10v brick

- Each brick supplies 10v to half of a Main Board
  - feed point of load regulators
- Board fabricated by vendor
- Burned in and tested at UTA
- NIU:
  - makes boxes
  - assembles with bricks
  - attaches ELMB MB
  - tests

box of 8 bricks



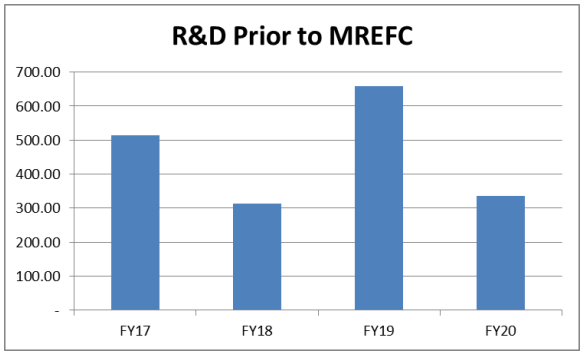


- Auxiliary Diode OR:

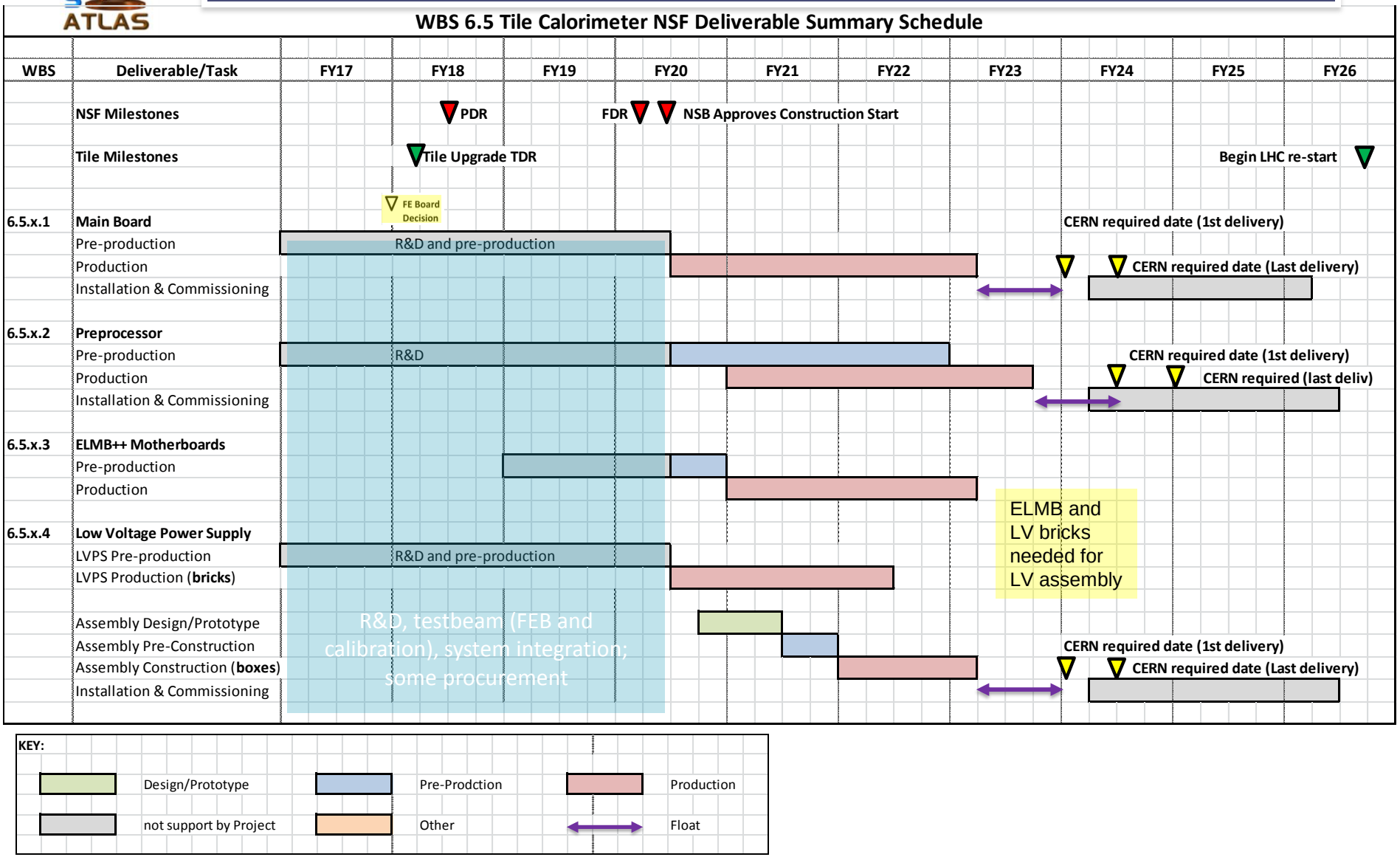
Research and Development

The Demonstrator Program

- R&D from USATLAS to build and evaluate demonstrators
  - 3in1, QIE front-end cards and Main Boards produced for demonstrator
  - LV, HV control boards designed and prototyped; LVboxes produced
  - Radiation certification of components and development of rad-hard optical modulator
- Good progress so far:
  - 2015: beam test of 3in1-based demonstrator (successful!)
  - 2016: two more beam tests to evaluate ASIC FEB's
  - 2016: simulations; which FEB handles pileup best?
  - 2017: experience with a demonstrator in ATLAS detector
  - 2017-2020: final integrated design, prototype, testing
    - Includes test beam running to measure Jet Energy Scale and radiation certification
- NSF MREFC funding start is FY20 Q3 ⇒ "R&D" includes some pre-production
  - total FY17-FY20/Q2 cost is $1,820k (construction cost on MREFC is $3,743k)



Level 4 Timeline



Cost and Effort Estimates

(more details in the BOEs)

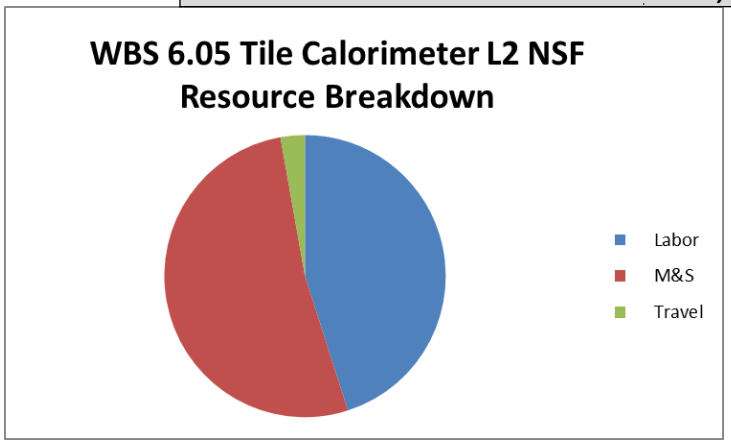
- The cost estimates are rather detailed and based on:
  - actual or similar Bill of Materials with quotes from vendors
    - assuming 20% discount from retail (our experience is more like 30-40%)
  - effort estimates based on the original construction, refined by the recent experience building and testing boards for the demonstrator
    - The FEB, Main Boards, LVPS bricks and boxes are very similar in production scope to the current versions … which we built!
    - The PreProcessor cards are new, ATCA technology, but we have the experience of constructing the demonstrator prototypes

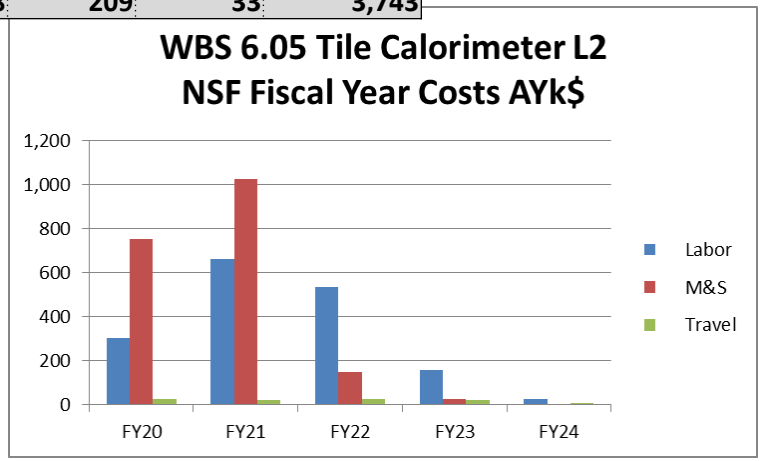
Total Cost vs FY

- front-loaded by procurement bulk purchases and test fixture construction
  - permits construction with ample float

6.05 Tile Calorimeter NSF Total Cost by Deliverable (AYk$)

Deliverable/Item	FY20	FY21	FY22	FY23	FY24	Total
Main Board	**592**	**856**	**277**	**32**	**33**	**1,790**
6.5.1.1 Main Board	592	856	277	32	33	1,790
Preprocessor	**65**	**258**	**228**	**57**	**0**	**608**
6.5.2.2 Preprocessor	65	258	228	57	0	608
ELMB++MB	**68**	**71**	**79**	**64**	**0**	**282**
6.5.3.3 ELMB++MB	68	71	79	64	0	282
LVPS	**360**	**523**	**124**	**56**	**0**	**1,063**
6.5.2.4 LVPS	264	320	82	0	0	665
6.5.4.4 LVPS Assembly	96	203	42	56	0	397
NSF Grand Total	**1,085**	**1,708**	**708**	**209**	**33**	**3,743**

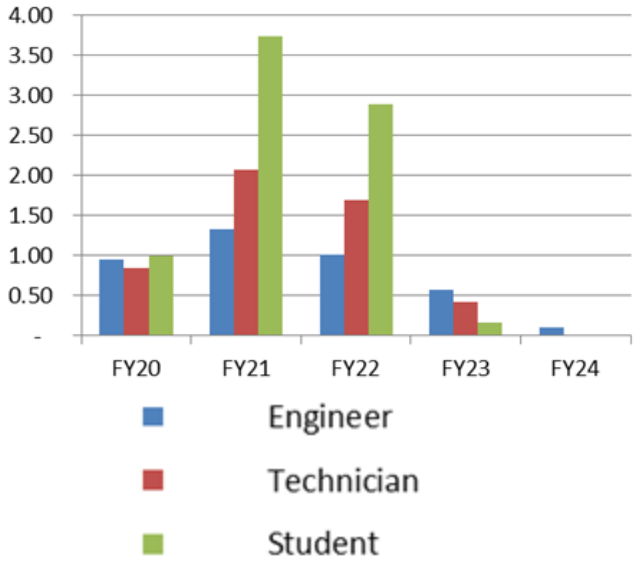




Labor Profile

6.05 Tile Calorimeter NSF Total FTEs by Deliverable (k$)						
Deliverable/Item	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Grand Total**
Main Board	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
6.5.1.1 Main Board	0.30	2.45	2.20	0.10	0.10	5.15
Preprocessor	**0.26**	**1.44**	**1.36**	**0.42**	**-**	**3.48**
6.5.2.2 Preprocessor	0.26	1.44	1.36	0.42	-	3.48
ELMB++MB	**0.45**	**0.37**	**0.47**	**0.35**	**-**	**1.64**
6.5.3.3 ELMB++MB	0.45	0.37	0.47	0.35	-	1.64
LVPS	**1.77**	**2.86**	**1.55**	**0.27**	**-**	**6.45**
6.5.2.4 LVPS	1.44	2.51	1.28	-	-	5.23
6.5.4.4 LVPS Assembly	0.34	0.35	0.27	0.27	-	1.22
NSF Grand Total	**2.78**	**7.12**	**5.59**	**1.14**	**0.10**	**16.73**

As these Tile projects are at universities, we benefit from low-cost labor by undergrads: it's good experience for them! They are qualified to monitor the burn-in and testing.



Risks

- Risks all low because of working demonstrator prototype
- Cost risk: very low
  - have BOMs from demonstrator; cost goes down for CERN bulk purchases
  - only assuming 20% bulk discount from retail (it's usually higher)
  - FPGAs likely to go down in cost, but we are using quotes for FY18
- Schedule risk: low
  - not negligible, because Tile installation is early in the schedule
  - but significant float in proposed schedule (12-19 months)
  - main risk: delivery of FEB, LV bricks from non-US institutes
- Technical risk: very low
  - Tile is in lower radiation area
  - electronics design not too sophisticated; often similar to current design
  - main risk: replacement component does not meet radiation standard

6.5 Risk Registry

HL-LHC Upgrade Project Risk Registry for L2 Systems January 4, 2016			Risk Evaluation (L/M/H)							
WBS	**Title**	**Risk Owner**	**Cost**	**Schedule**	**Scope**	**Contingency %**	**Contingency AYk$**	**Average Risk Score**	**Identified Risks (See BoEs)**	
6.5	**Tile Calorimeter**	**Oreglia, Mark**				**35%**	**1,310**	**2.5**		
6.5.1.1	Main Board	Oreglia, Mark	L	L	L	35%	626	2.0	*A higher failure rate necessitating more repair, or increased component costs. *late delivery of parts. *Components no longer radiation qualified	
6.5.2.2	Preprocessor	De, Kaushik	L	L	L	35%	213	2.0	*late delivery of parts. *change in parts costs	
6.5.3.3	ELMB++MB	Huston, J	L	L	L	35%	99	2.0	*late delivery of parts. *The ELMB++ is designed to be standard for all DCS communications	
6.5.x.4	LVPS	Brandt A., Charaborty D.	M	L	L	35%	372	3.0	*Transfer of production (from one institution to another) increases schedule uncertainty. *Labor costs less certain due to lack of experience with this production *Card component no longer rad qualified.	

Contingency

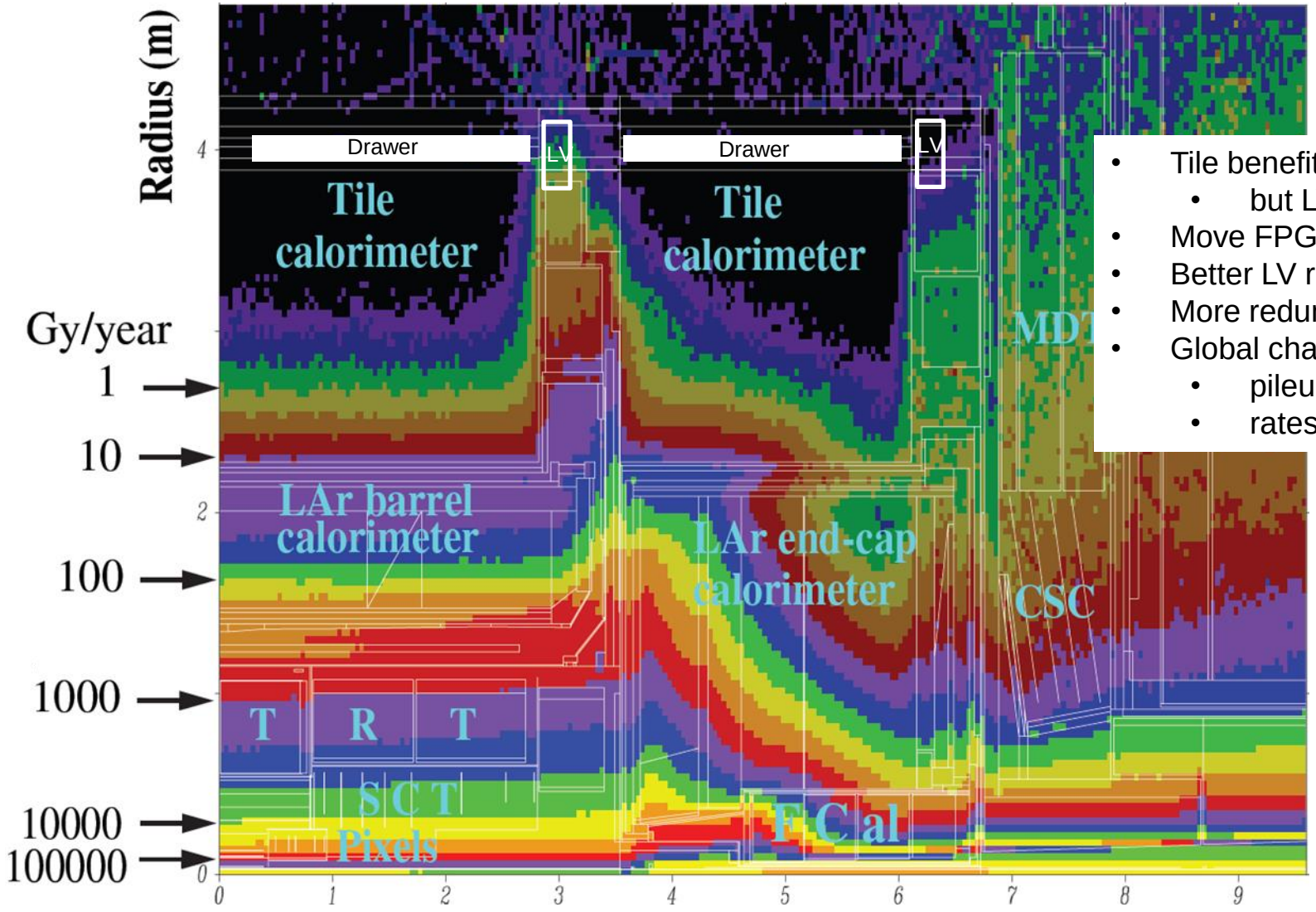
- Budget Contingency
  - Nominal 35% adequately covers the detail costing, verified by demonstrator program
- Scope Contingency
  - LV box/assembly production 6.5.4.4
    - most likely US task to find someone else to cover; recovers $397k (11%)
    - would need to make that decision in CY 2021
- Scope Opportunity
  - LVPS
    - US undertakes 50% production in current proposal
    - Would cost additional $1063K
  - MB, if 3in1 front-end board is not chosen
    - the ASIC MBs are simpler, cheaper; could use excess funding to contribute FEB test stands, etc

Closing Remarks

- US Deliverables: Main Boards, PPR TDAQi, DCS control, LVPS
  - developed by US groups with long-time involvement in Tile
  - already proven by Tile demonstrator project
    - costs and effort well understood ⇒ low risk and well within contingency
- Total construction cost of $3743K (w/o contingency)
  - 2.8% of total US projects
- Low risks; here are the main ones, all mitigable:
  - MB: new component not radiation tolerant
  - PPR: FPGA cost
  - ELMB motherboard: new component not radiation tolerant
  - LVPS: new component not radiation tolerant

Backup Slides

Old Radiation Map (100 fb^{-1})



- Tile benefits from shielding
  - but LVPS in n-plume
- Move FPGAs in more
- Better LV rad tolerance
- More redundancy
- Global challenges:
  - pileup: μ=140-200
  - rates, latency

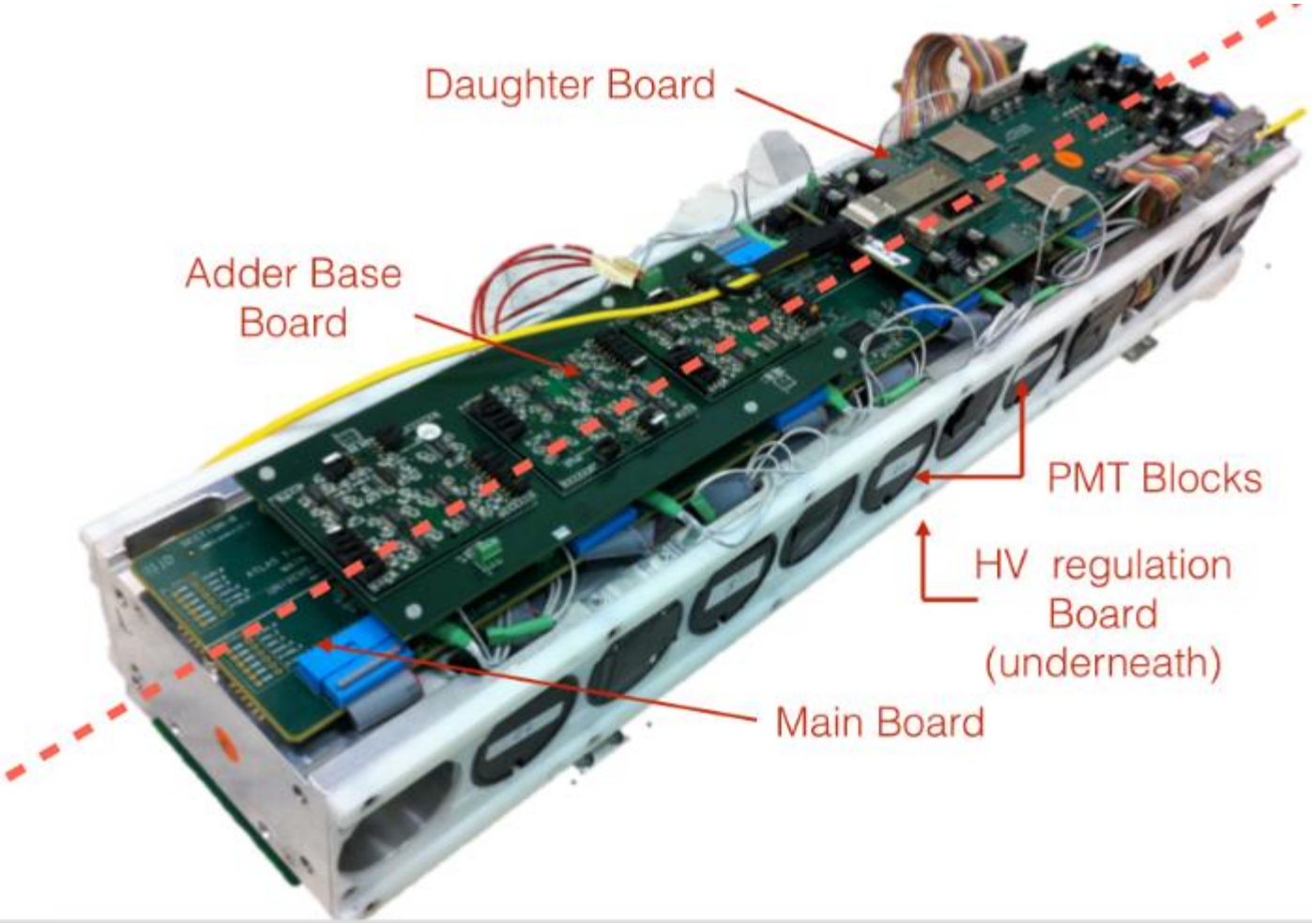
Front-end Alternatives

- Chicago's 3in1 FEB and associated Main Board are the **default**
  - Performing well in tests and radiation certification
  - Most complicated MB (has ADCs); total MB cost ≈ total FEB cost
  - Shapes pulse and has dual gain ranges
- Two ASIC alternatives being evaluated
  - QIE (ANL): boxcar integrator, 5 gain ranges
  - FATALIC (LPC Clermont-Ferrand): shaped pulse, 3 gain ranges
  - Downselect: by end of CY 2017
- Whatever alternative is chosen, UChicago and LPC will share:
  - Chicago makes the Main Boards (simpler for the ASIC alternatives)
  - LPC manufactures the front-end cards
    - This makes sense especially if an ASIC is used (single point of contact)

Level-4 Labor

6.05 Tile Calorimeter NSF Total FTEs by labor type						
Deliverable/Item/Labor Type	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Grand Total**
6.5.1 Tile_Chicago	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
6.5.1.1 Main Board	**0.30**	**2.45**	**2.20**	**0.10**	**0.10**	**5.15**
Engineer	0.10	0.50	0.40	0.10	0.10	1.20
Technician	0.20	0.95	0.80	-	-	1.95
Student	-	1.00	1.00	-	-	2.00
6.5.2 Tile_UTA	**1.70**	**3.95**	**2.64**	**0.42**	**-**	**8.71**
6.5.2.2 Preprocessor	**0.26**	**1.44**	**1.36**	**0.42**	**-**	**3.48**
Engineer	0.26	0.40	0.32	0.16	-	1.14
Technician	-	0.52	0.52	0.26	-	1.30
Student	-	0.52	0.52	-	-	1.04
6.5.2.4 Low Voltage Power Supply	**1.44**	**2.51**	**1.28**	**-**	**-**	**5.23**
Engineer	0.09	0.17	0.08	-	-	0.34
Technician	0.35	0.35	0.20	-	-	0.89
Student	1.00	2.00	1.00	-	-	4.00
6.5.3 Tile_MSU	**0.45**	**0.37**	**0.47**	**0.35**	**-**	**1.64**
6.5.3.3 ELMB++ Motherboards	**0.45**	**0.37**	**0.47**	**0.35**	**-**	**1.64**
Engineer	0.23	0.10	0.11	0.24	-	0.68
Technician	0.23	0.06	0.08	0.04	-	0.41
Student	-	0.21	0.28	0.07	-	0.56
6.5.4 Tile_NIU	**0.34**	**0.35**	**0.27**	**0.27**	**-**	**1.22**
6.5.4.4 LVPS Assembly	**0.34**	**0.35**	**0.27**	**0.27**	**-**	**1.22**
Engineer	0.27	0.16	0.09	0.07	-	0.58
Technician	0.07	0.19	0.09	0.11	-	0.46
Student	-	-	0.09	0.09	-	0.18
NSF Grand Total	**2.78**	**7.12**	**5.59**	**1.14**	**0.10**	**16.73**
Engineer	0.94	1.32	1.01	0.57	0.10	3.94
Technician	0.84	2.06	1.69	0.41	-	5.00
Student	1.00	3.73	2.89	0.16	-	7.78

A Demonstrator Mini-drawer



WBS Definitions 6.5.x.1,2

WBS #	WBS Title	WBS Dictionary	Level 2 Manager	Collaborating Institution	Funding Source
6.5	Tile Calorimeter	Replacement of readout and associated electronics for the Tile Calorimeter. US deliverables include: develoment of the Main Board, which houses front-end readout electronics; design and construction of data I/O transition modules for use with the Tile Pre-Processor boards; ELMB++ motherboards used in the collection of monitoring data from the detector and electronics; and production and assembly of the TileCal Low Voltage Power Supply system.	M. Oreglia (Chicago)	-	-
WBS #	WBS Title	WBS Dictionary	Deliverable PI	Collaborating Institution	Funding Source
6.5.1.1	Main Boards	This WBS covers the fabrication of main boards (MB) which manage the data flow, power distribution, monitoring, and calibrations of the Tile Calorimeter front-end electronics. This MB is more radiation tolerant than the current ones, which is a requirement for HL-LHC running. The deliverable for WBS 6.5.1.1 is production of 1,100 boards. Additional tasks are parts procurement and monitoring of outsourced assembly, elevated temperature burn-in of cards with testing and repair, and assembly on the "drawer" mechanical structure for acceptance testing at CERN.	M. Oreglia (Chicago)	Chicago	NSF
6.5.2.2	Preprocessor Interface Boards	This WBS covers the design and fabrication of the Trigger DAQ interface (TDAQi) blades which are the rear transition modules of the Tile calorimeter back-end preprocessor (PPR). These boards configure the processed data from the front-end electronics and route data to the DAQ system via the FELIX module and to the L0/L1 Calo and Muon trigger system through dedicated links. The deliverable for WBS 6.5.2.2 is production of 32 boards. Additional tasks are parts procurement and monitoring of outsourced assembly, burn-in of cards in a dedicated setup with validation testing and repairs when needed.	K. De (UTA)	UTA	NSF

WBS Definitions 6.5.x.3,4

WBS #	WBS Title	WBS Dictionary	Deliverable PI	Collaborating Institution	Funding Source
6.5.3.3	ELMB++Motherboard	This WBS covers the design and fabrication of the motherboard for the new ELMB++ board to be designed for the Tilecal HL-LHC running. The ELMB++ (and its motherboard) is an integral part of DCS control for the Tilecal. The plan is for the new ELMB++ board to allow for greater diagnostic capability for Low Voltage Power Supply failures. The new motherboard, which is mounted in the LV finger box, has to be capable of supporting those new features. The deliverables for WBS 6.5.3.3 are: (1) design of a new motherboard, (2) prototyping of that board, (3) design and production of test equipment for the motherboard, (4) production of 256 ELMB++ motherboards boards over a two-year period, and (5) follow-up of the integration of the ELMB++ motherboards in the Tilecal LVPS system. Items 1 and 2 are not part of project costs, but will be covered by prototyping/R&D funding. Additional tasks are parts procurement and monitoring of outsourced assembly, elevated temperature burn-in of cards with testing and repair.	J. Huston (MSU)	MSU	NSF
6.5.2.4, 6.5.4.4	Low Voltage Power Supply	This WBS covers the production of the Low Voltage Power Supply for the ATLAS Tile Calorimeter HLLHC upgrade. This version of the LVPS consists of +10 volt modules (bricks); 8 of these bricks are mounted in LVBOXes which are mounted at the end of each Tile Calorimeter drawer. 256 of these boxes are needed for the full calorimeter. The primary deliverable for WBS 6.5.2.4 is production of half (1040) of the total number of bricks and half (130) of the LVBOXes ; about 1,140 bricks are produced to account for anticipated yield of 90% over a two-year period. Additional tasks include parts procurement, PCB assembly (outsourced), testing of the bricks at standard and elevated temperature (Burn-in), and repair of faulty bricks. The bricks will be shipped to NIU for inclusion in boxes of eight, tested and shipped to CERN. A transition period from ANL to UTA including	A. Brandt (UTA) H. Hadavand (UTA) D. Charaborty (NIU)	UTA UTA NIU	NSF NSF NSF

The Bratislava Meeting

Tile IB agreed on upgrade interests 9/23/2015

Item	Intentions/Interests for production
Mini-drawers	Romanian cluster, IFAE, Clermont consulting
LVPS	UTA, Pisa, Prague AS and CU (ANL consulting), MSU (ELMB)
Active Dividers	To be found, Testbench to be handed by Clermont
FEB+MB	Chicago, Clermont shared In half in items (ANL consulting)
DaughterBoard	Stockholm
HV system	LIP, Prague AS and CU (to specify item) + Clermont help + ANL consulting(if HV opto)
TilePPr, i/f to TDAQ	Valencia, Wits, UTA
New DCS	LIP, MSU (also for ELMB developments)
PMT block	Dubna + to be found
PMTs robustness	Pisa, [Yerevan], UTA (have lifetime bench), Clermont
Optics	counters: Dubna, Wits, Protvino, CERN, MSU; fibers: LIP
MA-PMTs	Dubna, Minsk, CERN, Protvino, ANL(S.Ch), Pisa, MSU, UTA, synergies w/ ALFA
Laser system	Clermont (consulting), Pisa, LIP, CERN
Cs system	Protvino, CERN

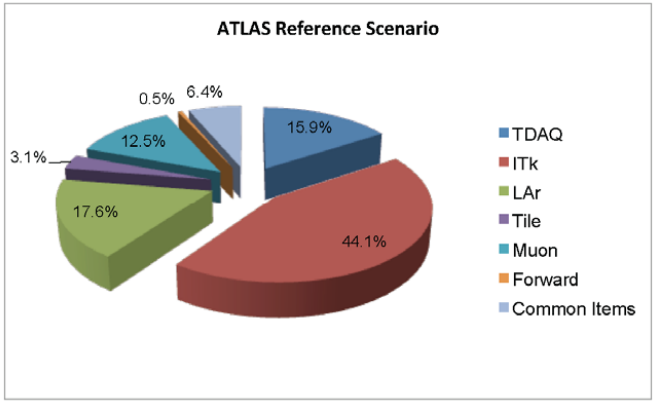
LVPS Considerations

- We decided to propose making 50% of the LV system because:
  - It brought the total US CORE to 20%
  - European colleagues expressed interest in participating
- History lessons:
  - Original bricks had high failure rate and SEU every pb^{-1}!
  - ANL had nothing to do with those, but created good redesign and manufactured replacements during LS1
  - ANL manufactured > 200 new style bricks for the demonstrator
    - Good knowledge of cost and procedures
- Transition: with ANL leaving Tile, UTA needs to learn the trade
  - $\Rightarrow$ ramp-up R&D funding by repairing bricks and building more for demonstrators

Cost Table from Scoping Document

Table 17. Tile Calorimeter Phase-II CORE costs.

WBS	Item	Base Cost [kCHF]	Option 1 [kCHF]	Option 2 [kCHF]	Option 3 [kCHF]
FE option:		3in1	3in1	QIE	AllInOne
HV option:		internal	external	internal	internal
Tile:		**8,580**	**8,785**	**8,987**	**8,619**
4.1	**Drawer Mechanics**				
4.1.1	Mini-drawers	1,229	1,229	1,229	1,229
4.1.2	Tools/Mechanics	60	60	60	60
4.2	**On-detector Electronics**				
4.2.1	PMT Dividers	173	173	173	173
4.2.2	FE Boards	716	716	1,852	873
4.2.3	Main Boards	987	988	258	869
4.2.4	Daughter Boards	1,561	1,561	1,561	1,561
4.2.5	LVPS System	987	987	987	987
4.2.6	HV System	768	973	768	768
4.3	**Off-detector Electronics**				
4.3.1	TilePPR	1,098	1,098	1,098	1,098
4.4	**Infrastructure**				
4.4.1	Services	1,001	1,001	1,001	1,001

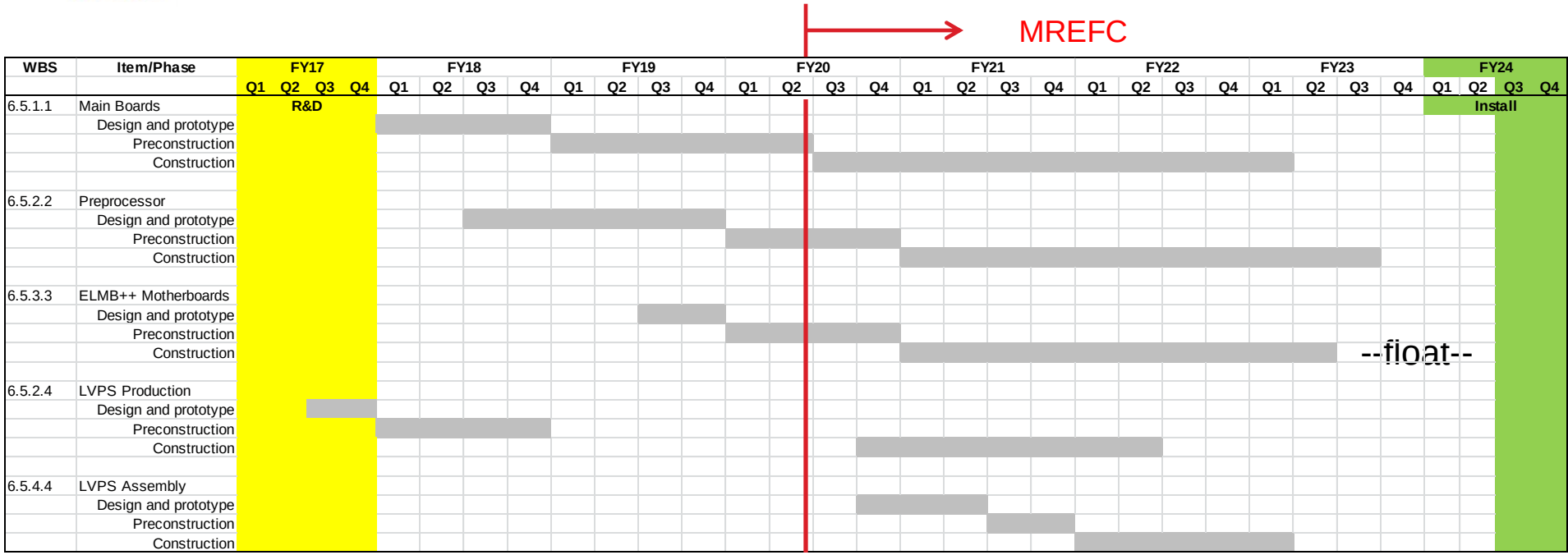


Exercise of 2015:
System managers refined LOI estimates

Most numbers reflect recent cost of building demonstrator

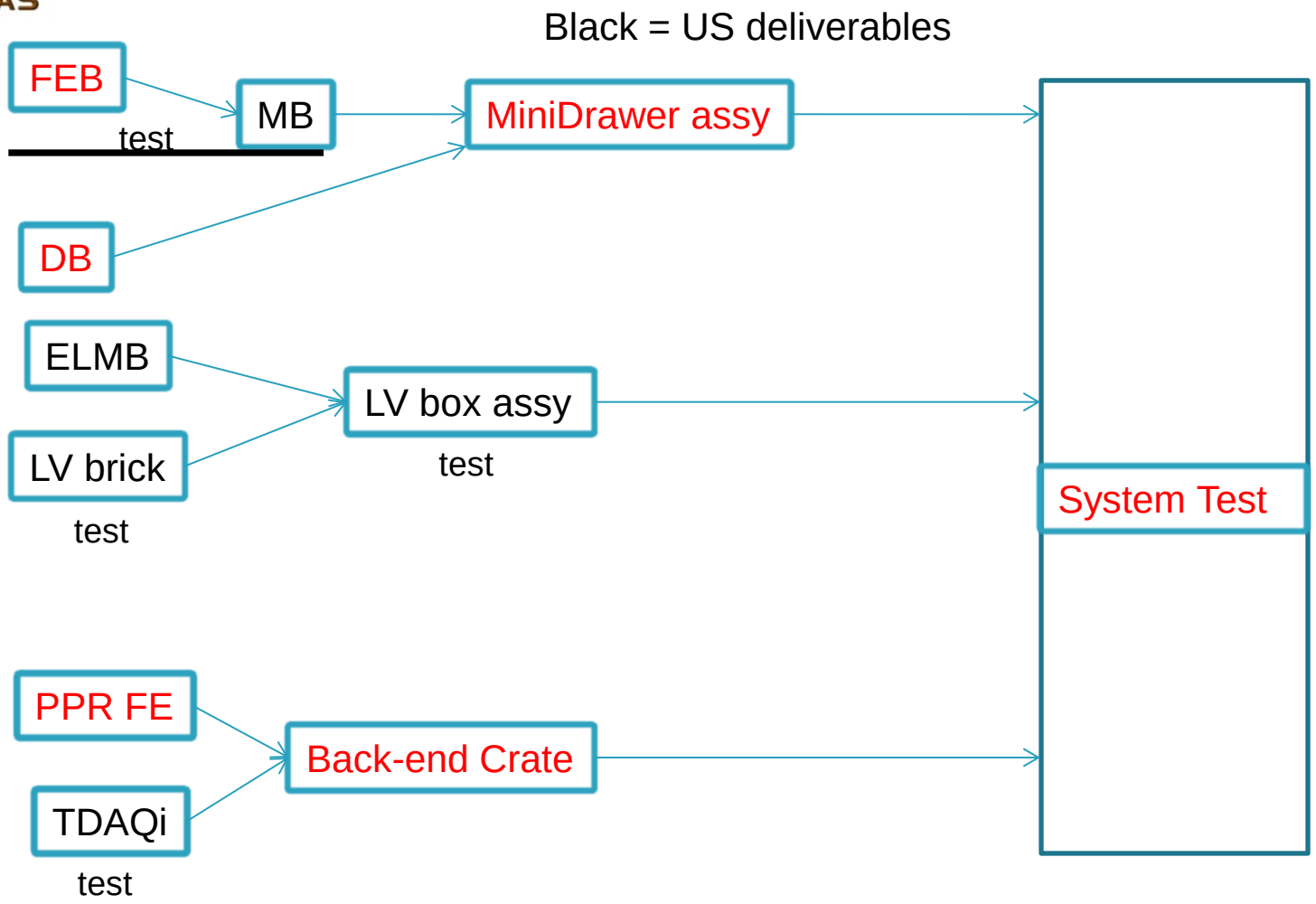
NB: omits some important items like system integration, shipping, etc

Project Phases

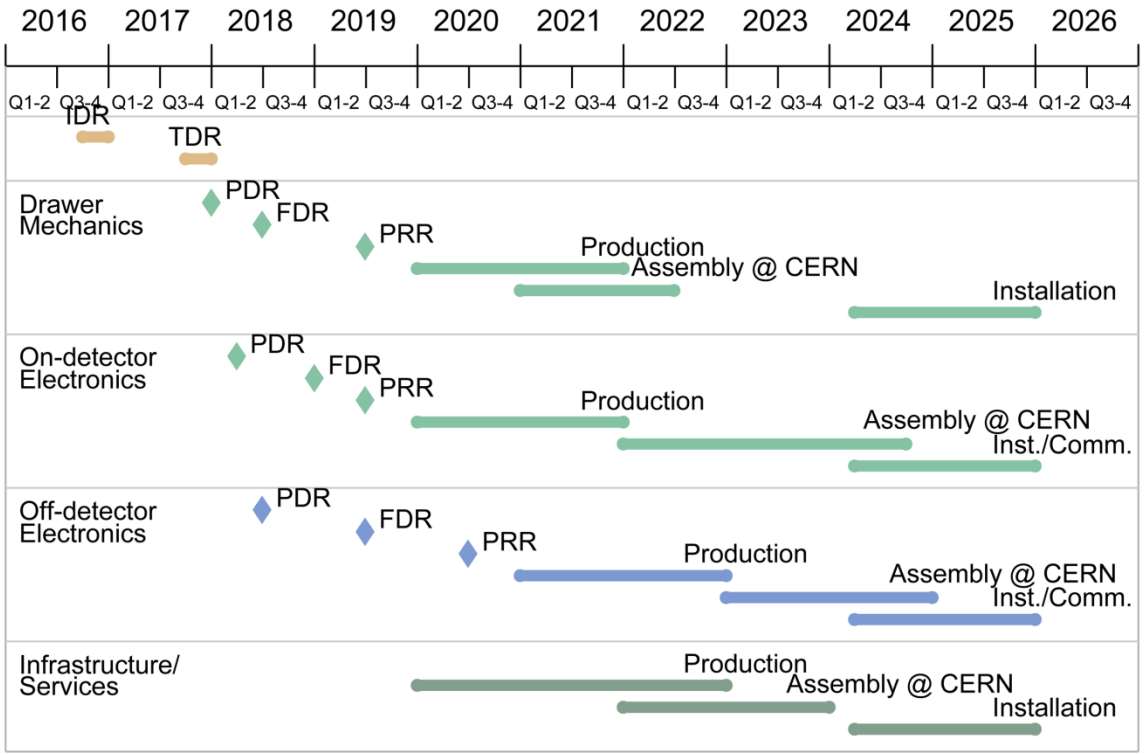


Note: length of gray band is not necessarily time needed to construct; there is waiting time for components or units from colleagues

Production Dependencies



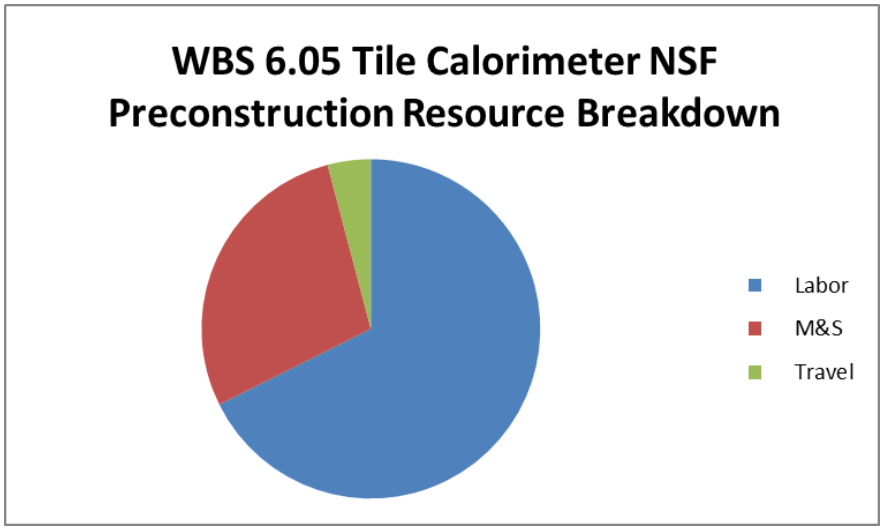
Schedule from Scoping Document

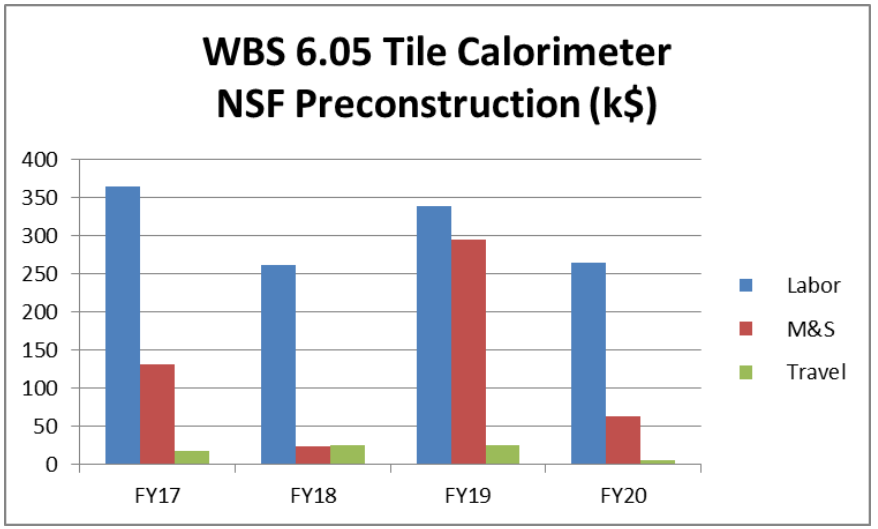


- This was an early exercise
- New "drop dead" dates: 6/30/2024 for all on-barrel electronics
  12/31/2024 for off-detector electronics

Pre-Construction Funding Profile

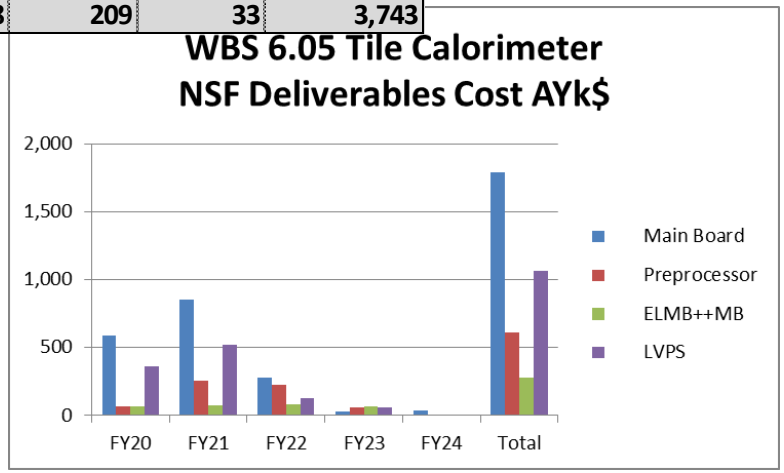
6.05 Tile Calorimeter NSF PreConstruction Cost (k$)					
	FY17	FY18	FY19	FY20	Grand Total
NSF					
Labor	365	262	339	265	1,231
M&S	131	24	295	64	514
Travel	18	26	25	6	75
NSF Total	**514**	**312**	**659**	**335**	**1,820**





Cost Profile by Subsystem

6.05 Tile Calorimeter NSF Total Cost by Deliverable (AYk$)						
Deliverable/Item	**FY20**	**FY21**	**FY22**	**FY23**	**FY24**	**Total**
Main Board	**592**	**856**	**277**	**32**	**33**	**1,790**
6.5.1.1 Main Board	592	856	277	32	33	1,790
Preprocessor	**65**	**258**	**228**	**57**	**0**	**608**
6.5.2.2 Preprocessor	65	258	228	57	0	608
ELMB++MB	**68**	**71**	**79**	**64**	**0**	**282**
6.5.3.3 ELMB++MB	68	71	79	64	0	282
LVPS	**360**	**523**	**124**	**56**	**0**	**1,063**
6.5.2.4 LVPS	264	320	82	0	0	665
6.5.4.4 LVPS Assembly	96	203	42	56	0	397
NSF Grand Total	**1,085**	**1,708**	**708**	**209**	**33**	**3,743**



6.05 Tile Calorimeter NSF Total Cost by Phase (AYk$)

Deliverable/Item/Phase	FY20	FY21	FY22	FY23	FY24	Grand Total
6.5.1 Tile_Chicago	**592**	**856**	**277**	**32**	**33**	**1,790**
6.5.1.1 Main Board	**592**	**856**	**277**	**32**	**33**	**1,790**
Production Procurement	456	456	0	0	0	912
Production PCB Assembly	136	137	0	0	0	274
Production Burn-in	0	175	180	0	0	355
Production Diagnose & Repair	0	37	38	0	0	75
Ship to CERN	0	20	27	0	0	47
Accceptance Test	0	31	31	32	33	127
6.5.2 Tile_UTA	**329**	**577**	**310**	**57**	**0**	**1,273**
6.5.2.2 Preprocessor	**65**	**258**	**228**	**57**	**0**	**608**
Pre-Prod Parts Procurement/QA	31	0	0	0	0	31
Pre-Prod PCB Assembly, QA	19	0	0	0	0	19
Pre-Prod Board Testing	15	0	0	0	0	15
Parts Procurement/Q&A	0	113	110	0	0	223
PCB Assembly, QA	0	17	4	0	0	21
Burn-in	0	63	52	24	0	139
Repairs	0	65	62	22	0	148
Shipping	0	0	0	12	0	12
6.5.2.4 Low Voltage Power Supply	**264**	**320**	**82**	**0**	**0**	**665**
Parts Procurement	119	122	0	0	0	240
PCB Fabr & Assy	67	61	0	0	0	128
Basic Checkout & Burn-in	54	92	50	0	0	196
Repairs	11	20	19	0	0	50
Management	11	22	11	0	0	44
Shipping	2	3	2	0	0	7
6.5.3 Tile_MSU	**68**	**71**	**79**	**64**	**0**	**282**
6.5.3.3 ELMB++ Motherboards	**68**	**71**	**79**	**64**	**0**	**282**
Pre-Prod Burn-in, Test & Repair	68	0	0	0	0	68
Parts Procurement/Q&A	0	42	42	0	0	84
Burn-in/Test/Repair	0	27	33	59	0	120
Shipping	0	3	4	4	0	11
6.5.4 Tile_NIU	**96**	**203**	**42**	**56**	**0**	**397**
6.5.4.4 LVPS Assembly	**96**	**203**	**42**	**56**	**0**	**397**
Pre-Prod Procurement	63	0	0	0	0	63
Pre-Prod Assembly	11	0	0	0	0	11
Pre-Prod Burn-in, Test & Repair	15	0	0	0	0	15
Pre-Prod Diagnostics & Repair	7	0	0	0	0	7
Test Equipment	0	64	0	0	0	64
Production Procurement	0	139	0	0	0	139
Production Assembly	0	0	11	2	0	14
Production Burn-in/Checkout	0	0	14	14	0	28
Production Diagnose & Repair	0	0	17	18	0	35
Shipping	0	0	0	22	0	22
NSF Grand Total	**1,085**	**1,708**	**708**	**209**	**33**	**3,743**